IN THE SPECIFICATION:

Please amend and replace the paragraph beginning on line 12 of page 12 in the Specification as follows:

As illustrated, the read row pointer 30 and the read row pointer 36 each indicate the next available physical register pointer that is available for assignment as a destination operand of a logical register. The read row ~~portion~~ pointer 30 corresponds to the second portion 22 of the structure and the read row pointer 36 corresponds to the first portion 20 of the structure. The write row pointer 32 and the write row pointer 38 each indicate where a physical register pointer should be written for a physical register holding an operand value corresponding to a logical register soon to be overwritten by an instruction in the pipeline and thus become a free register once that instruction is retired. The write row pointer 32 corresponds to the second portion 22 of the structure and the write row pointer 38 corresponds to the first portion 20 of the physical register list 14. The retire row pointer 34 and the retire row pointer 40 point to in each of their respective portions 22 and 20 of the physical register list 14, the physical register pointer of a physical register assigned to an instruction that is the next instruction to be retired by the microprocessor 10.

Please amend and replace the paragraph beginning on line 13 of page 16 in the Specification as follows:

If during the update the read row pointer 30 comes within a predetermined number of rows of the retire row pointer 34, a stall condition exists (step 56 in Figure 3). The stall condition exists

when the read row pointer 30 gets too close to the retire row pointer 34 indicating that the available region 26 may be too small to provide an adequate number of destination registers for the next set of instructions. Consequently, the microprocessor 10 stalls, meaning that it stops fetching instructions until more registers are added to the available region 26. To cure the stall condition, the microprocessor 10 allows instructions in the pipeline to retire, which advances the retire row pointer 34 towards the write row pointer 32 and away from the read row pointer 30 (step 58 in Figure 3). When enough instructions have retired to make the available region 26 sufficiently large, the microprocessor 10 may continue to fetch new instructions and the stall condition concludes. The predetermined distance typically corresponds to the number of instructions the microprocessor 10 can fetch in a single cycle. In the illustrative embodiment, the predetermined unsafe distance between the read row pointer 30 and the retire row pointer 34 is eight rows because the microprocessor 10 can fetch of up to eight instructions in a single cycle. If there is a sufficient number of rows between the read row pointer 30 and the retire row pointer 34 a stall condition does not exist and the physical register pointers in the available region 26 may be read and allocated as destination operand locations for logical registers (step ~~52~~ 62 in Figure [[3]] 4).